REMARKS

Claims 1-3, 6-14, and 17-19 are pending in the present application. Claims 4-5, 15-16, and 20-43 were previously cancelled. No claims have been amended herein. No new matter has been added. Applicants respectfully request reconsideration of the claims in view of the following remarks.

Claims 1-3, 6-7, 9-14, and 17-18 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Matsumoto et al. (U.S. Patent No. 6,455,894 B1, hereinafter "Matsumoto") in view of Paton et al. (U.S. Patent Application Publication No. 2002/0111021 A1, hereinafter "Paton"). Applicants respectfully traverse these rejections.

Claim 1 recites at least one of the distinguishing features of the present invention, namely, "a first dummy silicide structure . . . formed completely over an isolation region, the isolation region comprising a dielectric material in a recess in the semiconductor substrate." The Office Action asserts that the substrate recited in Applicants' claim 1 is disclosed by the combination of the silicon layer 3, the buried insulating film 2, and silicide regions 10c and 10d of Matsumoto, and that the isolation region recited in Applicants' claim 1 is disclosed by the dummy gate insulating film 4c of Matsumoto. This is simply incorrect.

First, the dummy gate *insulating* film 4c is not an *isolation* region, which is known in the art to isolate active areas from each other. Rather, the dummy gate insulating film 4c is a gate dielectric layer that is formed along a surface of an active area of the silicon layer 3. Applicants note that "isolation" regions have a meaning in the art to refer to structures used to isolate devices such as transistors. *See, e.g.*, Wolf, S.,

Silicon Processing for the VLSI Era, Volume 2 – Process Integration, p. 12, a copy of which is attached hereto. The isolation regions of Matsumoto correspond to isolating film 5a "formed between the MOS transistors TR1 in order to electrically *isolate* the elements." Matsumoto, column 1, lines 62-64. Accordingly the dummy gate insulating film 4c, which is positioned on an active area, cannot be considered an isolation region as recited in Applicants' claim 1.

Second, it should be noted that Applicants' claim 1 explicitly recites that the isolation region is formed in a recess in the semiconductor substrate. One of ordinary skill in the art will realize that that the dummy gate insulating film 4c is formed by depositing an oxide over the surface of the silicon layer 3. After the silicon layer 3 is patterned, drain regions and source regions are formed and a silicide process is performed to form the silicide regions 10c and 10d. *See, e.g.*, Matsumoto, column 1, lines 31-61. Thus, the dummy gate insulating film 4c is formed on a planar surface of the silicon layer 3, and only afterwards, the silicide regions 10c and 10d are formed on opposing sides of the dummy gate insulating film. Accordingly, the silicide regions 10c and 10d cannot be considered part of the substrate in which the isolation region is formed as recited in Applicants' claim 1.

Claim 13 also recites at least one of the distinguishing features of the present invention, namely, "at least one dummy silicide structure formed completely on the isolation region, the at least one dummy silicide structure comprising a silicide layer and a dielectric layer, the dielectric layer being a separate layer from the isolation region." The Office Action asserts that the dummy silicide structure recited in Applicants' claim

13 is disclosed by the combination of the dummy gate electrode 7c, the silicide region 9c, and the interlayer insulating film 11. This is simply incorrect.

First, the dummy gate *insulating* film 4c is not an *isolation* region as asserted by the Office Action. As discussed above, the dummy gate insulating film 4c is part of the device rather than an isolation region that separates devices.

Second, the structure of Matsumoto the Office Action asserted as disclosing Applicants dummy silicide structure is not "formed completely on the isolation region" as recited in Applicants' claim 13. The Office Action identified as part of the dummy silicide structure the interlayer insulating film 11. As clearly illustrated in Figure 41 of Matsumoto, for example, the interlayer insulating film 11 extends beyond the dummy gate insulating film 4c, which the Office Action asserted was the isolation region. Even assuming that the dummy gate insulating film 4c is an isolation region, which it is not, the interlayer insulating film 11 cannot be said to be formed completely on the dummy gate insulating film 4c when the interlayer insulating film 11 extends over the entire substrate.

Applicants note that if the Examiner is interpreting "completely on" to mean that it completely covers the dummy gate insulating film 4c, then the silicide region 9c is not "completely on" the dummy gate insulating film 4c. Applicants' claim 13 recites that the dummy silicide structure is "completely on" the isolation region. So, under what interpretation of "completely on" are both the silicide region 9c and the interlayer insulating film 11, both of which the Office Action asserts make up the dummy silicide structure of Applicants' claim 13, "completely on" the dummy gate insulating film 4c? Clearly, only the silicide region 9c is "completely on" the dummy gate insulating film 4c.

Accordingly, the interlayer insulating layer may not be considered part of the dummy silicide structure.

Claims 2, 3, and 6-12 depend from claim 1 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claims 14 and 17-19 depend from claim 13 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claims 1, 8, 13, and 19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsumoto in view of Nakamura (U.S. Patent No. 5,739,574, hereinafter "Nakamura"). Applicants respectfully traverse these rejections.

The Office Action's rejection of claim 1 fails to present a prima facie case of obviousness. The Office Action merely asserted in paragraph 2 that claim 1 was obvious over Matsumoto in view of Nakamura, but failed to provide any support or motivation. Accordingly, Applicants respectfully request that the rejection of claim 1 under 35 U.S.C. § 103(a) be withdrawn.

Similarly, the Office Action's rejection of claim 13 fails to consider all of the recited limitations. For example, the Office Action fails to consider that the dummy silicide structure comprises "a silicide layer and a dielectric layer, the dielectric layer being a separate layer from the isolation region." As discussed above, Matsumoto fails to disclose this limitation, and Nakamura fails to fix this deficiency. Accordingly, Applicants respectfully request that the rejection of claim 13 under 35 U.S.C. § 103(a) be withdrawn.

Claims 8 and 19 depend from and further limit claims 1 and 13, respectively. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

In view of the above, Applicants respectfully submit that this response complies with 37 C.F.R. § 1.116. Applicants further submit that the claims are in condition for allowance. No new matter has been added by this amendment. If the Examiner should have any questions, please contact Applicants' attorney at the number listed below. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

July 14, 2008
Date

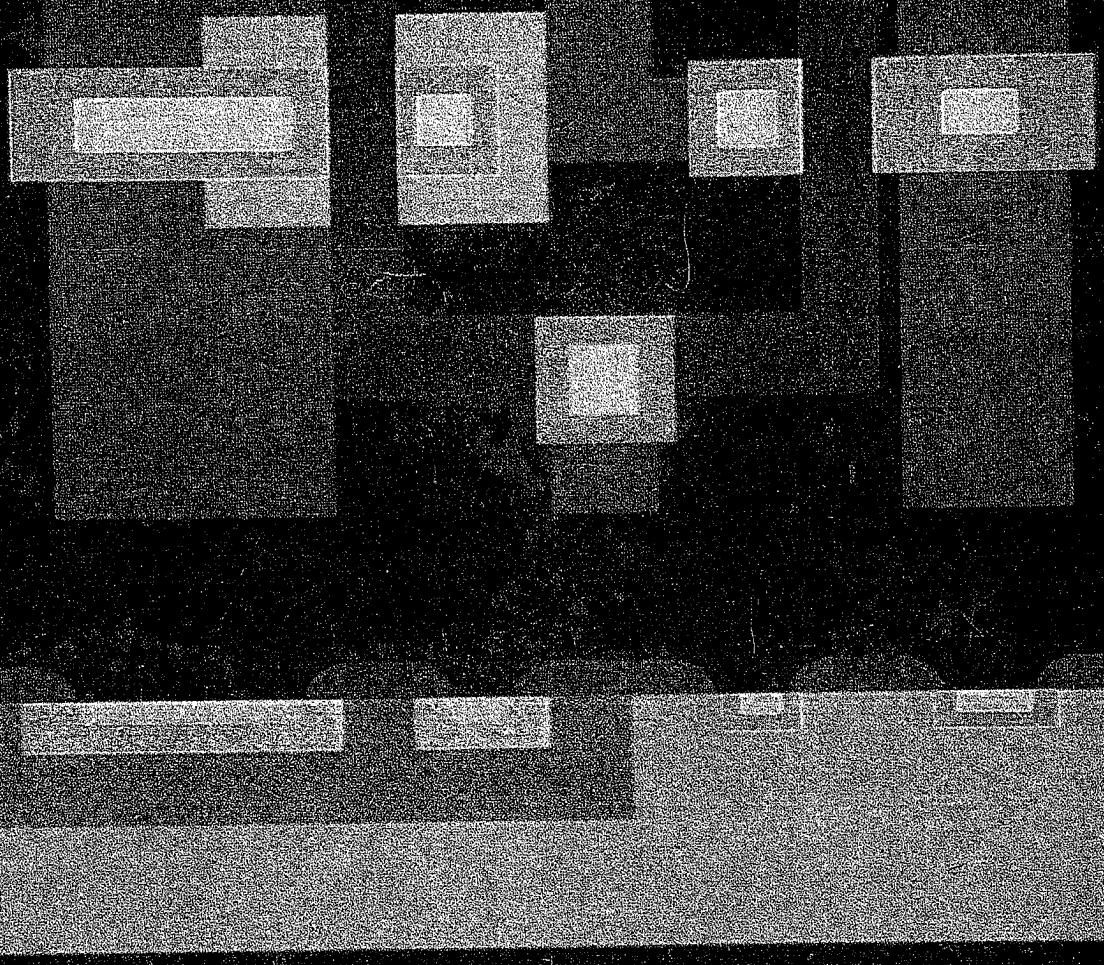
/Roger C. Knapp/
Roger C. Knapp
Reg. No. 46,836
Attorney for Applicants

SLATER & MATSIL, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, TX 75252
Tel: 972-732-1001
Fax: 972-732-9218

Silicon Processing

for the VLSI Era

Volume 2 - Process Integration



S. Wolf

SILICON PROCESSING

FOR

THE VLSI ERA

VOLUME 2:

PROCESS INTEGRATION

STANLEY WOLF Ph.D.
Professor, Department of Electrical Engineering
California State University, Long Beach
Long Beach, California

LATTICE PRESS

Sunset Beach, California

CHAPTER 2

ISOLATION TECHNOLOGIES FOR INTEGRATED CIRCUITS

Implementing electric circuits involves connecting *isolated* devices through specific electrical paths. When fabricating silicon integrated circuits it must therefore be possible to isolate devices built into the silicon from one another. These devices can subsequently be interconnected to create the specific circuit configurations desired. From this perspective, we can see that isolation technology is one of the critical aspects of fabricating integrated circuits.

A variety of techniques have been developed to isolate devices in integrated circuits. One reason is that different IC types (e.g., NMOS, CMOS, and bipolar) have somewhat different isolation requirements. Furthermore, the various isolation technologies exhibit differing attributes, with respect to minimum isolation spacing, surface planarity, process complexity, and density of defects generated during fabrication of the isolation structure. Tradeoffs can be made among these characteristics when selecting an isolation technology for a particular circuit application. This chapter surveys the various isolation technologies, including their evolution up to those being evaluated for submicron devices.

Before the invention of integrated circuits, only discrete diodes, bipolar transistors and field-effect transistors (FETs) could be fabricated. In the early 1950s, these discrete devices exhibited relatively high reverse-bias junction leakages and low breakdown voltages (caused by the large density of traps at the surface of single-crystal silicon).

In 1958, a group of workers at Bell Telephone Laboratories, led by Atalla, found that when a thin layer of SiO_2 was grown on the surface of silicon where a *pn* junction intercepts the surface, the leakage current of the junction was reduced by a factor from 10 to 100. It was later understood that the oxide reduces and stabilizes many of the interface and oxide traps. Not only did such oxide-passivation of the silicon surfaces allow diodes and transistors to be fabricated with significantly improved device characteristics, but the leakage path along the surface of the silicon was also effectively shut off. Thus, one of the fundamental isolation capabilities needed for planar devices and integrated circuits had also been developed. In his report on the evolution of the MOS transistor, C. T. Sah remarks that the successful effort by the Bell Labs group to stabilize Si surfaces was the most important technological advance in microelectronics

during the 1950s, and that it blazed the trail that led to the development of the silicon integrated circuit.[90]

With the advent of integrated circuits, it became necessary to provide electrical isolation between devices fabricated on the same piece of silicon. Since bipolar ICs were the first to be developed, a technology for isolating the collector regions of the bipolar devices was also the first to be invented (termed *junction isolation).*

PMOS and NMOS ICs did not need junction isolation, but it was still necessary to provide an isolation structure that would prevent the establishment of parasitic channels between adjacent devices. The most important technique developed was termed *LOCOS isolation* (for LOCal Oxidation of Silicon), which involved the formation of a semirecessed oxide in the nonactive (or *field*) areas of the substrate.

Eventually, bipolar ICs adopted a similar LOCOS-isolation technology (with the oxide performing a somewhat different function than in MOS circuits). The nature of CMOS also required that isolation exist between devices in adjacent tubs as well as between devices within each tub.

As device geometries reached submicron size, conventional LOCOS isolation technologies reached the limits of their effectiveness, and alternative isolation processes for CMOS and bipolar technologies were needed. Modified LOCOS processes (which overcome some drawbacks of conventional LOCOS for small-geometry devices), trench isolation, and selective-epitaxial isolation, were among the newer approaches adopted.

Devices that must function under high voltages and in harsh radiation environments require even more stringent isolation techniques. These techniques are generally referred to as *silicon-on-insulator* (SOI) isolation methods. They include such older approaches as *dielectric isolation* (DI) and *silicon-on-sapphire* (SOS), as well as more recently developed technologies, such as *separation by implanted oxygen* (SIMOX), *zone-melting-recrystallization* (ZMR), *full isolation by porous-oxidized silicon* (FIPOS), and *wafer bonding*. These technologies will be described in the final sections of the chapter.

2.1 BASIC ISOLATION PROCESSES FOR BIPOLAR ICs

2.1.1 Junction Isolation

As mentioned in the introduction, isolation techniques for bipolar ICs were the first to be developed. To see why isolation is needed in bipolar ICs consider Fig. 2-1a, which shows several non-isolated bipolar transistors on a monolithic substrate. It can be seen that all the collector regions are electrically connected through the substrate - obviously, an unacceptable circumstance for all bipolar IC structures (except those few in which common collectors are desired). To circumvent this problem, several approaches to isolating the devices have been developed.

The most important isolation technique used in early bipolar ICs is *junction isolation*, and it has been incorporated as part of the *standard buried collector* (SBC) process (described in this section as well as in chap. 7), the *triple diffused (3D)* process